What is Claimed is:

1.   For the testing of the operation of processing unit, a system for identifying the occurrence of a plurality of events in a processor unit, the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream;

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream; and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals;

wherein the program counter trace apparatus is responsive to plurality of simultaneous event signals, the program counter trace apparatus generating multiple-event sync marker signal group identifying the occurrence of the plurality of simultaneous events and relating the event signals to the timing trace stream and the program execution.

2.   The system as recited in claim 1 wherein the marker signal group includes a program counter address, a timing index and a periodic sync ID.

1   3.   The system   as   recited   in   claim   1   further

2   comprising:

3   data trace apparatus responsive to signals from the

4   processing unit, the data trace apparatus generating a data

5   trace stream, wherein the periodic sync ID signals are

6   applied to the data trace apparatus provide periodic sync

7   markers in the data trace stream; and

8   a host processing unit, the host processing unit

9   responsive to the timing trace stream, the program counter

10   trace stream and the data trace stream, the host processing

11   unit   reconstructing   the   processing   activity   of   the

12   processing unit from the trace streams.

13

14   4.   The method for communicating an occurrence of a

15   reset signal from a target processor unit to a host

16   processing unit, the method comprising:

17   generating a timing trace stream, a program counter

18   trace stream, and data trace stream, and

19   in the program counter trace stream, including a

20   marker signal group indicating a simultaneous occurrence of

21   a plurality of event signals and relating the occurrence to

22   the data trace stream, to the timing trace stream, and to

23   the program execution.

24

25   5.   The   method   as   recited   in   claim   4   further

26   including:

1   in the marker signal group, including a periodic sync

2 ID, a timing index and a program counter address.

3

4   6.   In a processing unit test environment wherein a

5 target processor transmits a plurality of trace streams to

6 a host processing unit, a marker signal group included in a

7 trace signal stream, the marker signal group comprising:

8   indicia of the simultaneous occurrence of a plurality

9 of event signals;

10   indicia of the relationship of the occurrence of the

11 reset signal to the target processor clock; and

12   indicia of the relationship of the occurrence of the

13 event signals to the target processor program execution.

14

15   7.   In a target processing unit generating trace test

16 signals for transfer to a host processing unit, program

17 counter trace generation apparatus comprising:

18   a storage unit;

19   a decoder unit responsive to a rest signal for storing

20 a signal group identifying a first event signal in the

21 storage unit in a first location in the storage unit, the

22 decoder unit generating a control signal, the decoder unit

23 generating a second control signal when multiple

24 simultaneous events are identified;

25   a gate unit responsive to the control signal, the gate

26 unit transmitting processor signals applied thereto to the

27 storage unit for storage at defined locations, the signals

1   stored in the storage unit forming a portion of a multiple-
2   event sync marker;

3   a multiple-event gate unit responsive to the second
4   control signal for storing indicia of additional event
5   signals in the storage unit; and

6   a FIFO unit coupled to the storage unit, the FIFO unit
7   receiving the multiple-event sync marker when the multiple-
8   event sync marker has been assembled, the FIFO unit
9   transferring the multiple-event sync marker to the host
10 processing unit.

11

12   8.   The program counter trace apparatus as recited in
13 claim 7 wherein the signals applied to the gate unit
14 include a program counter address, a periodic sync ID, and
15 a timing index.

16

17   9.   The program counter trace apparatus as recited in
18 claim 8 wherein the multiple-event sync marker signal
19 includes a plurality of packets.

20

21   10. The program counter trace apparatus as recited in
22 claim 7 wherein the sync markers in the FIFO unit are
23 transferred from the unit in response to third control
24 signals.